

M62364FP

8-bit 8ch Multiplying D/A Converter with Buffer Amplifiers

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Description

The M62364FP is a CMOS 8-bit 8ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by the simple three-wiring method (DI, CLK, LD).

The output buffer amplifiers operating in AB-class has both sinking and driving capabilities of 1.0 mA or more and can operate in a whole supply range from V_{DD} to GND.

The IC is suitable for a use in automatic adjustment applications in conjunction with a MCU by utilizing the terminal D_0 for a cascading connection.

Features

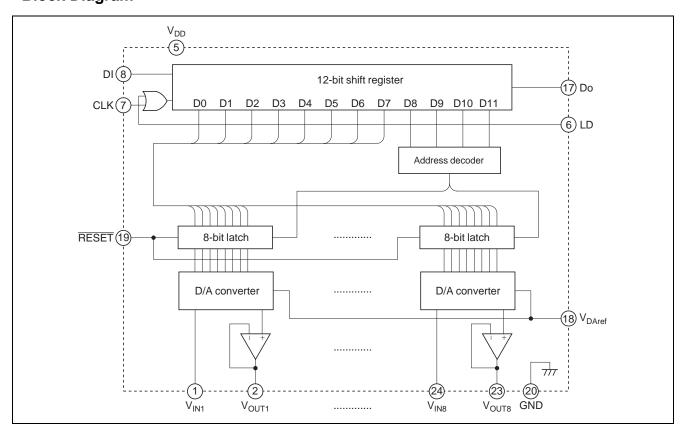
- Three-wiring serial data transmission
- Doubled precision 8ch D/A converter employing an R-2R with higher-order segment method
- 8 buffer amplifiers operating in a whole supply voltage range from V_{DD} to GND
- 4 quadrant multiplication

Application

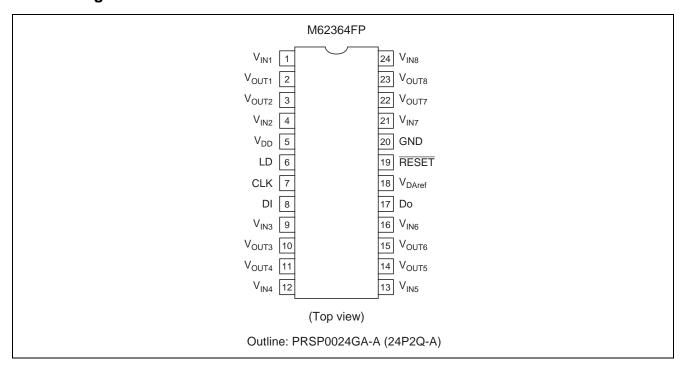
Digital to analog conversion for consumer and industrial equipment.

Gain setting and automatic adjustment of display-monitor and CTV.

Block Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
8	DI	Serial data input
17	Do	Serial data output
7	CLK	Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge of the clock.
6	LD	A low state enables data loading to the 12-bit shift register.
		During a rising edge of LD, the data will be loaded to the output register.
19	RESET	Reset 8-bit latches
2	V _{OUT1}	D/A converter output with 8-bit resolution
3	V _{OUT2}	
10	V _{OUT3}	
11	V _{OUT4}	
14	V _{OUT5}	
15	V _{OUT6}	
22	V _{OUT7}	
23	V _{OUT8}	
5	V_{DD}	Power supply
20	GND	Ground
1	V _{IN1}	D/A converter input
4	V _{IN2}	
9	V _{IN3}	
12	V _{IN4}	
13	V _{IN5}	
16	V _{IN6}	
21	V _{IN7}	
24	V _{IN8}	
18	V _{DAref}	D/A converter reference voltage input

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.3 to +7.0	V
Digital input voltage	V _{IND}	-0.3 to +7.0	V
Analog input voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V
Analog output voltage	V _{OUT}	-0.3 to V _{DD} + 0.3	V
D/A reference voltage	V _{DAref}	-0.3 to V _{DD} + 0.3	V
Operating temperature	Topr	-20 to +75	°C
Storage temperature	Tstg	-40 to +125	°C

Electrical Characteristics

<Ana/Dig Common Part>

 $(V_{DD} = 5 \text{ V} \pm 10\%, V_{DD} \ge V_{IN}, \text{GND}, V_{DAref} = 0 \text{ V}, \text{Ta} = -20 \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.})$

			Limits			
Item	Symbol	Min	Тур	Max	Unit	Conditions
Supply voltage	V_{DD}	2.7	5.0	5.5	V	
Supply current	I _{DD}	_	_	3.5	mA	CLK = 1 MHz, V_{CC} = 3 V, I_{AO} = 0 μA

<Digital Part>

 $(V_{DD} = 5 \text{ V} \pm 10\%, V_{DD} \ge V_{IN}, \text{ GND}, V_{DAref} = 0 \text{ V}, \text{ Ta} = -20 \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.})$

			Limits			
Item	Symbol	Min	Тур	Max	Unit	Conditions
Input leak current	I _{ILK}	-10	_	10	μΑ	$V_{IN} = 0$ to V_{DD}
Digital input "Low" voltage	V _{IL}	_	_	$0.2~V_{DD}$	V	
Digital input "High" voltage	V _{IH}	0.8 V _{DD}	_	_	V	
Do terminal output "Low" voltage	V _{OL}	_	_	0.4	V	I _{OL} = 2.5 mA
Do terminal output "High" voltage	V _{OH}	$V_{DD} - 0.4$	_	_	V	$I_{OH} = -400 \mu A$

<Analog Part>

 $(V_{DD} = 5~V \pm 10\%,~V_{DD} \geq V_{IN},~GND,~V_{DAref} = 0~V,~Ta = -20~to~+85^{\circ}C,~unless~otherwise~noted.)$

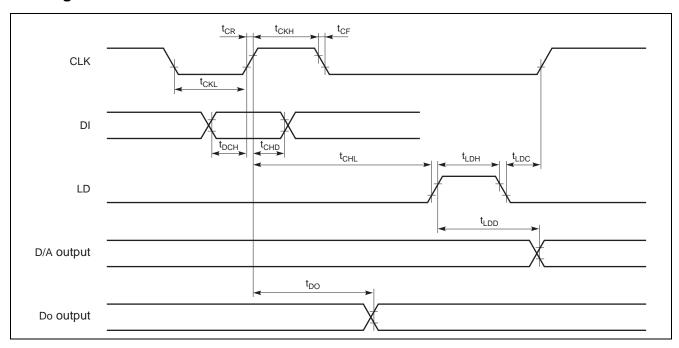
			Limits			
Item	Symbol	Min	Тур	Max	Unit	Conditions
Input current	I _{IN}	_	_	0.30	mA	$V_{\text{IN}} = 5 \text{ V}, V_{\text{DAref}} = 0 \text{ V}$ Proportional to Max. input current condition $(V_{\text{IN}} - V_{\text{DAref}})$ and digital data of each channels
D/A reference input current	I _{DAref}	-2.40	_	_	mA	V_{IN} = 5 V, V_{DAref} = 0 V Proportional to Max. input current condition ($V_{IN} - V_{DAref}$) and digital data of each channels
Resolution	RES	_	8	_	bit	
Differential nonlinearity	DNL	-1	_	1	LSB	V _{DAref} = 0.050 V (10 mV/LSB)
Nonlinearity	NL	-1	_	1	LSB	Without load ($I_{AO} = \pm 0$)
Buffer amplifier output	V _{AO}	0.1	_	V _{CC} - 0.1	V	$I_{AO} = \pm 100 \ \mu A$
voltage range		0.2	_	V _{CC} - 0.2		$I_{AO} = \pm 500 \ \mu A$
Buffer amplifier output current range	I _{AO}	-1	_	1	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Output capacitive load	Co	_	_	0.1	μF	
Buffer amplifier output impedance	Ro	_	5	_	Ω	

AC Characteristics

 $(V_{DD} = 5~V \pm 10\%,~V_{DD} \geq V_{IN},~GND,~V_{DAref} = 0~V,~Ta = -20~to~+85^{\circ}C,~unless~otherwise~noted.)$

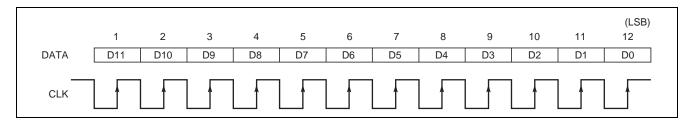
		Limits				
Item	Symbol	Min	Тур	Max	Unit	Conditions
Clock "L" pulse width	t _{CKL}	200	_	_	ns	
Clock "H" pulse width	tckH	200	_	_	ns	
Clock rise time	t _{CR}	_	_	200	ns	
Clock fall time	t _{CF}	_	_	200	ns	
Data setup time	t _{DCH}	60	_	_	ns	
Data hold time	t _{CHD}	100	_	_	ns	
LD setup time	t _{CHL}	200	_	_	ns	
LD hold time	t _{LDC}	100	_	_	ns	
LD "H" pulse duration time	t _{LDH}	100	_	_	ns	
Data output delay time	t _{DO}	70	_	350	ns	C _L = 100 pF
D/A output setting time	t _{LDD}	_	_	300	μS	$C_L \le 100 \text{ pF}, \text{ V}_{AO}: 0.1 \leftrightarrow 2.6 \text{ V}$
						This time until the output becomes the final value of 1/2 LSB

Timing Chart



Digital Data Format

12-bit serial data



Data Assignment

D0	D1	D2	D3	D4	D5	D6	D7	: DAC data
(LSB)							(MSB)	•
D8	D9	D10	D11	: DAC se	elect data			

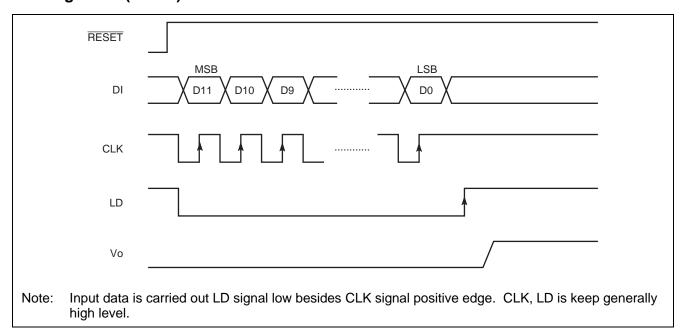
DAC Data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	V _{DAref}
1	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 1 + V_{DAref}$
0	1	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 2 + V_{DAref}$
1	1	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 3 + V_{DAref}$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	(V _{IN} - V _{DAref}) / 256 × 255 + V _{DAref}

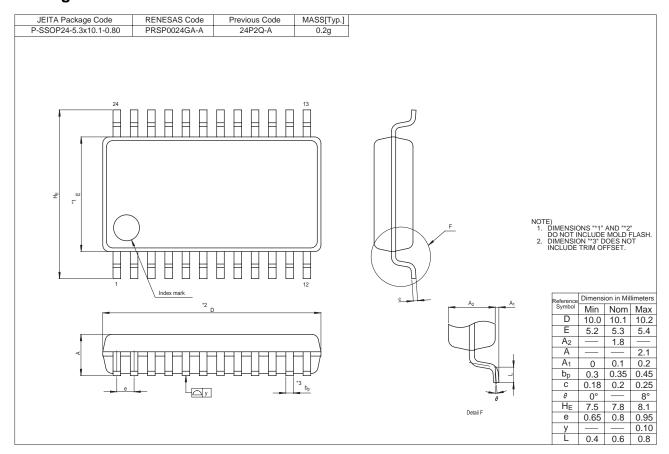
DAC Select Data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	V _{OUT1} selection
0	0	1	0	V _{OUT2} selection
0	0	1	1	V _{OUT3} selection
0	1	0	0	V _{OUT4} selection
0	1	0	1	V _{OUT5} selection
0	1	1	0	V _{OUT6} selection
0	1	1	1	V _{OUT7} selection
1	0	0	0	V _{OUT8} selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)



Package Dimensions



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